ARMY RESEARCH LABORATORY

User-based Software Tool for S-parameter Conversion and Manipulation

by Scott Trocchia, Dr. Tony Ivanov, and Dr. Robert Proie

ARL-TR-5650 **September 2011**

NOTICES

Disclaimers

The findings in this report are not to be construed as an official Department of the Army position unless so designated by other authorized documents.

Citation of manufacturer's or trade names does not constitute an official endorsement or approval of the use thereof.

Destroy this report when it is no longer needed. Do not return it to the originator.

Army Research Laboratory
Adelphi, MD 20783-1197

ARL-TR-5650 **September 2011**

User-based Software Tool for S-parameter Conversion and Manipulation

Scott Trocchia, Dr. Tony Ivanov, and Dr. Robert Proie
Sensors and Electron Devices Directorate, ARL

REPORT DOCUMENTATION PAGE	Form Approved OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED (From - To)
September 2011	Final	June to August 2010

4. TITLE AND SUBTITLE
User-based Software Tool for S-parameter Conversion and Manipulation

5a. CONTRACT NUMBER

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
Scott Trocchia, Dr. Tony Ivanov, and Dr. Robert Proie

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
U.S. Army Research Laboratory
ATTN: RDRL-SER-E
2800 Powder Mill Road
Adelphi MD 20783-1197

8. PERFORMING ORGANIZATION REPORT NUMBER
ARL-TR-5650

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

13. SUPPLEMENTARY NOTES

14. ABSTRACT
S-parameters fully characterize the linear behavior of an arbitrary number of ports. We aim to characterize various field-effect transistors (FETs), each having a certain gate width and geometry, from their S-parameters. We extract the data from the vector network analyzer in real-time and perform a series of calculations and conversions on the initial S-parameters. Using a software tool written in C++ that interfaces with the vector network analyzer (VNA), the corresponding computer monitor, and two direct current (DC) power supplies, the user can collect relevant real-time data about a device under test (DUT). The software contains a number of user-input interfaces paired with appropriate graph canvases. Its main functionalities include: conversion of S-parameters to H-parameters, selection of H_{21} in an effort to calculate the frequency (f_t) at which the transistor exhibits unity current gain, a family of current-voltage (I-V) curves of the DUT, and calculations and plots of transconductance (g_m). Future work will include measuring a variety of devices and allowing the software tool to collect statistics on them.

15. SUBJECT TERMS
S-parameter, conversion, H2I, graphical user interface

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Scott M. Trocchia
Unclassified	Unclassified	Unclassified	UU	22	19b. TELEPHONE NUMBER (*Include area code*) (301) 394-0728

Contents

List of Figures

1. Introduction/Background

Field Effect Transistors (FETs) are three-terminal devices consisting of a gate, drain, and source. By applying voltage across the gate to source terminal (V_{GS}), sweeping the voltage across the drain to source terminal (V_{DS}), one may observe the drain to source current (I_{DS}) for any given FET device. Plotting this current-voltage (I-V) relationship with V_{DS} on the x-axis and I_{DS} on the y-axis, one can see the DC characteristics of the FET device and one can tell whether or not a transistor functions at various gate to source voltages. This concept serves as the foundation for logically determining other radio frequency (RF) properties of the FET, such as maximum unity gain (f_T), the frequency point at which the H_{21} gain transitions from positive to negative, and f_{MAX}, the maximum frequency at which the transistor can exhibit any type of power gain. By using the DC characteristics of the FET, the user can obtain accurate S-parameter readings and measurements of the FET device at different DC operating points, namely varying values of V_{DS} and V_{GS}.

The collection of the DC and RF characteristics for a given FET is necessary to facilitate circuit design. Using common measurement tools known as a vector network analyzer (VNA) and several DC power supplies, one can efficiently measure the I-V characteristics and the S-parameters for a given FET. Interfacing software to control the measurement tools, one can measure, construct, and analyze the DC and RF characteristics, namely the I-V plots, H_{21}, f_T, and f_{MAX} in real-time. Additionally, devices can be characterized and parameters, such as gate voltage, drain voltage, and number of points to be graphed, can be changed with the simple click of a few buttons. Overall, consolidation of these qualities into one finite set of graphical user interfaces (GUIs) helps the user visualize the measured and interpreted results. The engineer, knowing the values collected from the provided software tool, can uniquely characterize a device under test (DUT) and implement further circuit designs.

2. Operating Instructions

Four essential screens comprise the software tool. The first screen that appears upon execution of the program is the menu selection screen (figure 1), which depicts three user choices and should be used to pull up the other three sets of screens. Before beginning to look at the electrical features of one given FET, the user must input the known V_{GS} and V_{DS} boundaries. The user enters these boundary conditions, applies a small voltage (V_{GS}), and ensures that the device is passing I_{DS} current and is therefore operational.

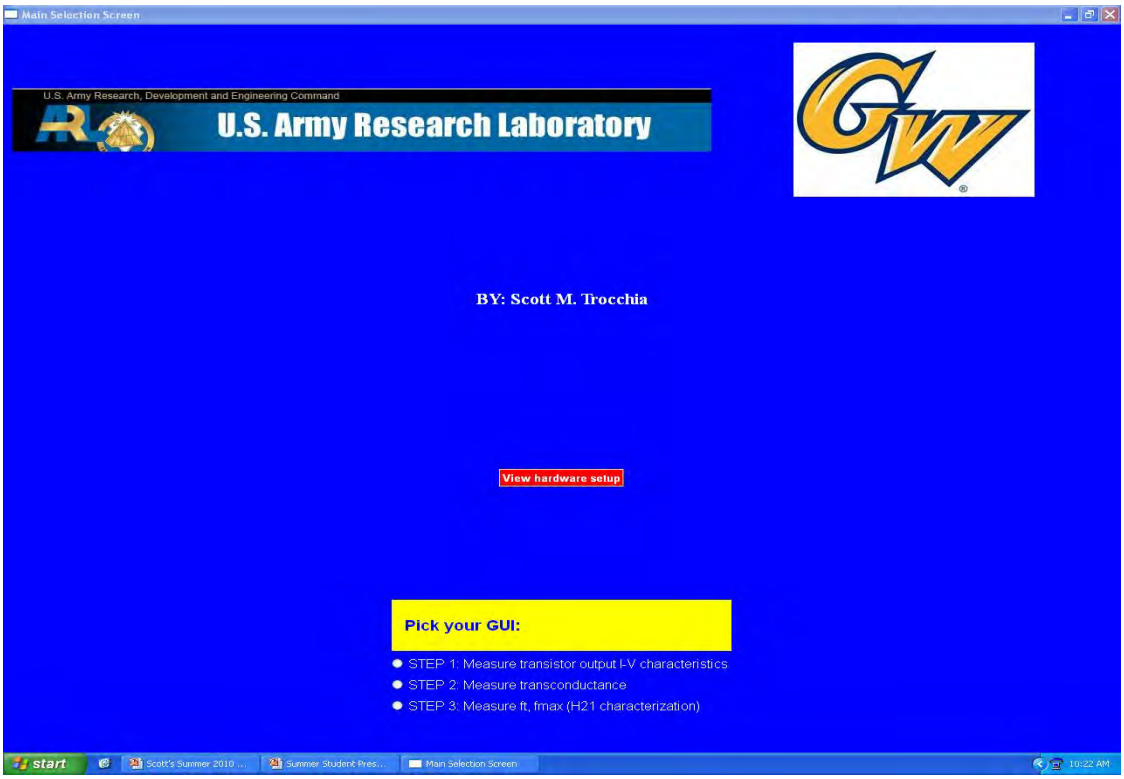

Figure 1. Main selection screen.

2.1 Measuring I-V Curves

The user begins measuring the DC characteristics of a FET by clicking on the radio button labeled: "STEP 1: Measure transistor output I-V characteristics". The steps are numbered so that, in practice, the user will follow them in the prescribed order. This action will minimize the main screen and load two separate windows: a graph canvas and a user interface (UI), where the user can input relevant bias conditions into the proper text fields. Notable bias conditions include a range of V_{GS} and a fixed V_{DS}. Both parameters are arbitrary, yet through sufficient experimentation, the user can get a feel for which values produce acceptable output curves. Note that the user can minimize or maximize the main screen at his or her discretion. In total, there are eleven windows that pop up; users can access each of them through a series of button presses.

2.2 Measuring Transconductance

Once the user becomes satisfied with the graphed family of output curves, thereby verifying proper functionality of the DUT, the user can move on to collecting transconductance information. One can initiate this process by clicking on the "STEP 2: Measure transconductance" radio button on the main screen. This portion of the software suite includes two GUIs—one for the user input and one for the graphical output—as well. The user would enter a fixed V_{DS} that has the same magnitude as in the I-V analysis. With the push of a button, the user will be presented with a split panel graphical view. On the left-hand side appears one graphical canvas containing two curves. One of those curves is a V_{GS} versus I_{DS} plot, and the

other curve is its time derivative; the latter curve is, by definition, the transconductance. The right graph is a zoomed in version of the left graph which depicts the derivative curve in isolation.

This pair of graphs serves to inform the user of two pieces of information: the dependent variable, the peak g_m value in units of millisiemens, and the independent variable, the gate-source voltage corresponding to that peak. The user should take note of these values, along with the values from the I-V analysis, for all parameters output in UIs are useful in the last evaluation phase.

2.3 Measuring and Analyzing S-parameters

This last evaluation involves looking at the H_{21} parameter to characterize the frequency behavior of the DUT. This study is, from the user's perspective, more complicated because there are many windows to navigate. The user would access this GUI set by simply clicking on the radio button labeled "STEP 3: Measure ft, fmax (H21 characterization)" on the main screen. One UI and one graph canvas pop up. The user can then load in saved files of calibrated standards, or they can measure them in real-time when they are conducting an experiment. The standards used are one open circuit, two shorts, and one through. They represent parasitic capacitances of the substrate of the DUT and are necessary for better calibration techniques. Known calibration methods only factor in error calculations up until the probe tips, but with the calculations provided by my software tool, full de-embedding is accomplished. After a successful loading sequence, the user may enter the optimal biases V_{DS} and V_{GS} marked down from the previous two steps.

Four graphs subsequently appear in the graph canvas: H_{21}, which was extracted from S_{21}, $G_{TU\ max}$, the maximum unilateral transducer power gain, U, the unilateral power gain, and G_{ma}, the maximum available stable power gain. The first item is useful for computing f_T; the next three are useful for calculating f_{MAX}. Simultaneously, five GUIs (four UIs and one graph canvas) appear. In three out of four of those UIs, the user would type in a frequency range representing sections of a particular curve which appear most linear to him or her. The GUI environment would dynamically change, and users would see a regression line overlaying each corresponding data set. From the regression line's intersection with the x-axis, f_T and f_{MAX} values are now known. Those values are conveniently extracted and shown in the last small UI.

For all of the analyses considered, results can be saved to a text file in any valid file directory. The graphs will not appear because graphs cannot be formatted properly within the text file, but the data off which the graphs are based can be saved and archived. With regards to the frequency characterization in step three, all data and associated regression lines can be saved.

3. Hardware Setup

Hardware drives the fundamental operation of this experimental setup. A generic setup for the software described to properly operate is shown in figure 2: a probe station with DC or RF proves used to bias the device (depending on the device), a network analyzer to study S-parameters outputted from the probes, and two DC power supplies, one to sweep voltage and the other to collect current. All equipment must daisy chain to the same GPIB (General Purpose Interface Bus) in order for them to communicate with one another. This is essential, for if mutual communication is not guaranteed, any given experiment fails from the onset.

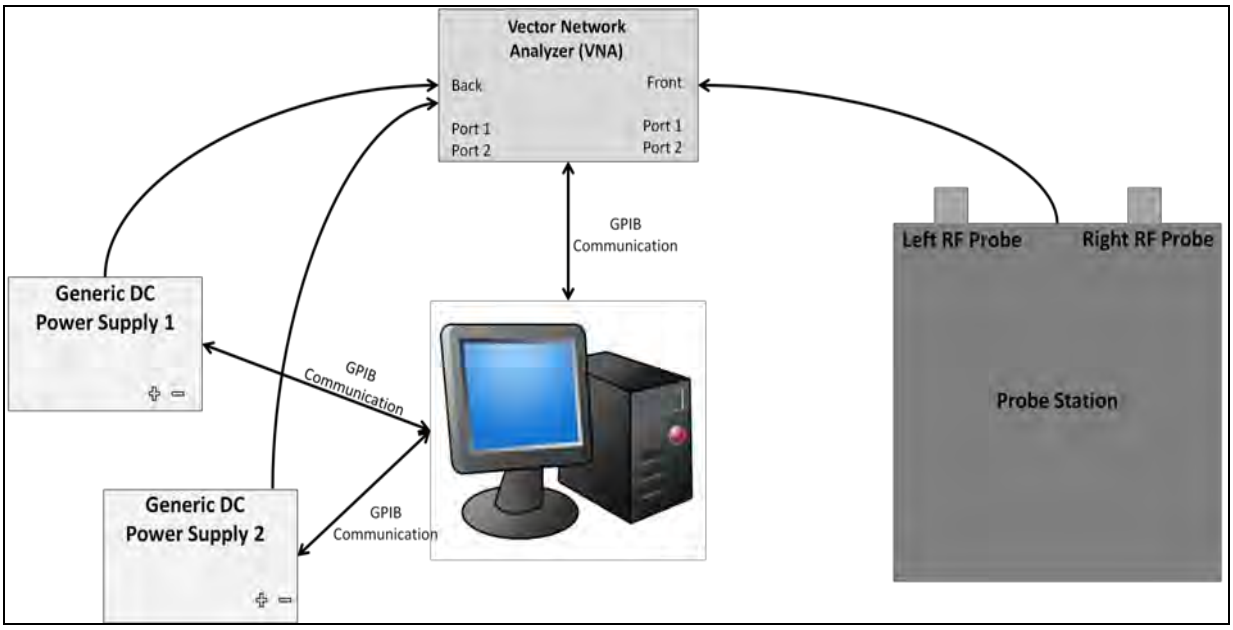

Figure 2. Equipment setup and configuration.

The preferred hardware setup employed one Agilent E3645A (GPIB: 2) and one Keithley 2400 (GPIB: 5) DC power supply; the former measured drain-to-source voltage and the latter recorded gate-to-source voltage. The positive terminal of the Agilent's supply connected to the rear Port 2 of an Agilent E8361C PNA Microwave Network Analyzer; the Keithley's positive terminal coupled to Port 1 on the back. The source of the FET and the negative terminal of each instrument were grounded. Both RF probes, each with a ground-signal-ground (GSG) pad configuration, linked to the front connection ports of the PNA – the left one to Port 1 and the right one to Port 2. The appropriate apparatus can be located in lab bay 3D067 of Building 207.

If the user understands the necessary components, he or she can open the executable file and start collecting data. Each step discussed in the previous section is associated with an algorithm.

Additionally, calculations are embedded within the C++ code. Once the hardware is properly setup, the calculations and displaying of results can now be automated.

4. Software Architecture

This section is provided for those wishing to understand the programmatic portion of this work. The casual user may be less interested and may skip this section without losing any information. The flow chart shown in figure 3 details the algorithm implemented in this characterization software. The premise for the family of output curves is simple: sweep the drain voltage for one particular gate voltage; after each sweep, increment the gate voltage by one and perform the drain sweep again. Repeat until the maximum drain voltage has been reached.

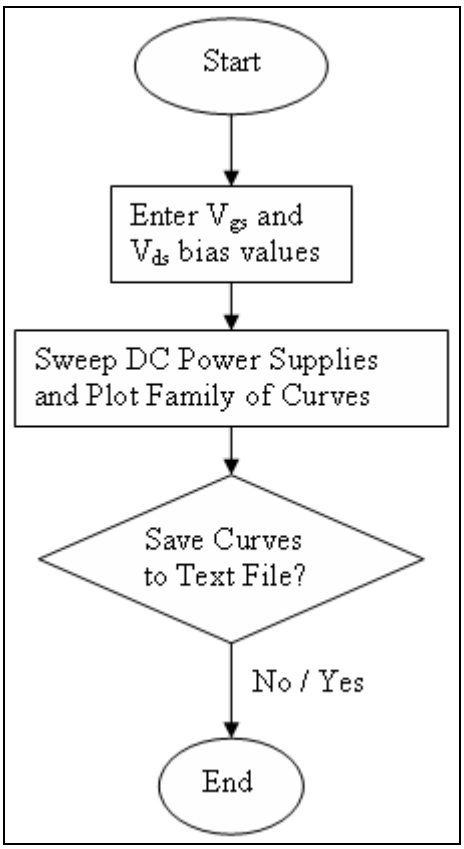

Figure 3. I-V algorithm flow chart.

The transcondutance computational algorithm (figure 4) resembles the I-V algorithm. The steps are virtually the same, but where the two differ is in the plotting (V_{GS} on the x-axis compared to V_{DS} on the x-axis in the I-V plots) and saving options. The algorithm is: ground the source terminal of the DUT; sweep the gate voltage on one power supply while maintaining a fixed drain voltage on the other supply.

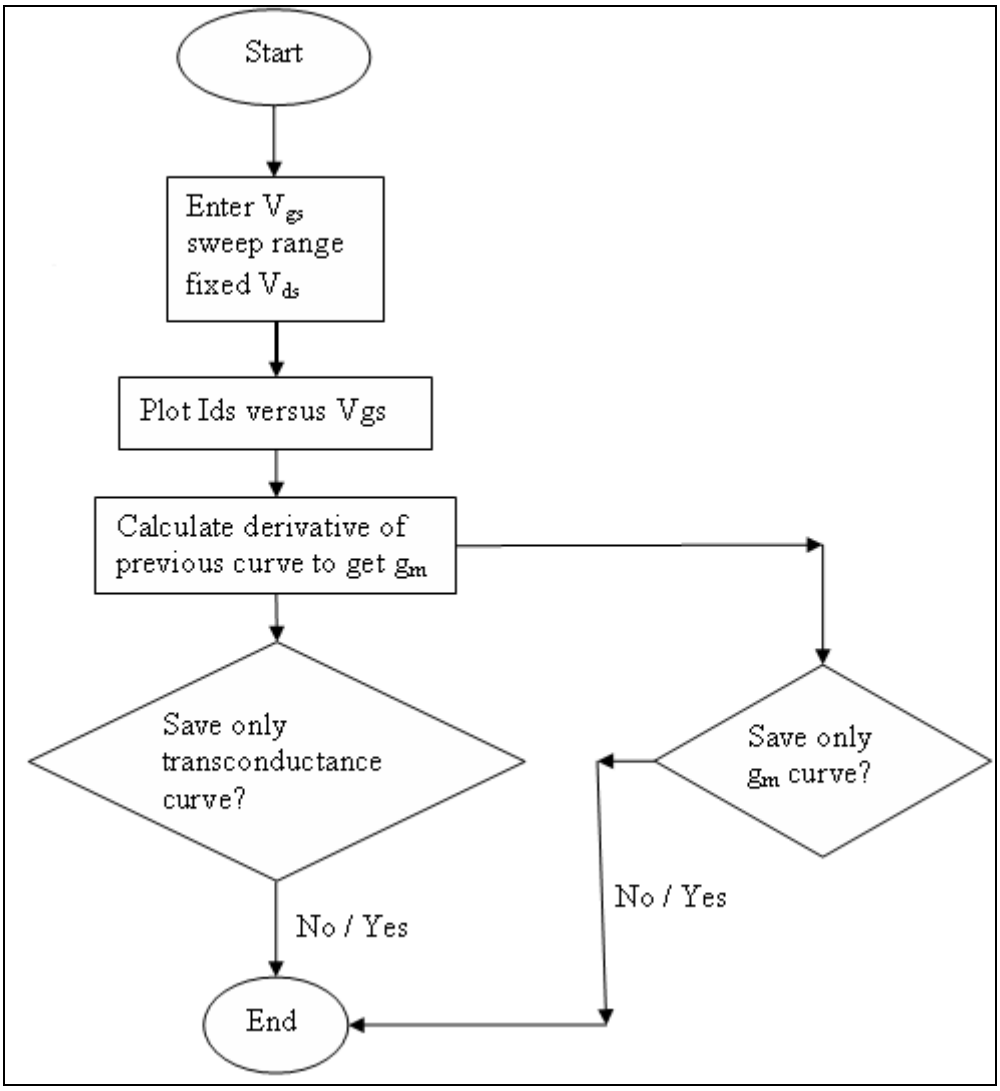

Figure 4. Transcondutance algorithm flow chart.

The H_{21} algorithm is exceedingly more complicated. In this scenario, it abides by this flow (figures 5 and 6): submit V_{DS} and V_{GS} biases, de-embed the DUT at its terminals, and convert S-parameters to H-parameters. This scheme is fully implemented in this project is the method outlined by Vandamme (*1*). The inclusion of different de-embedding algorithms such as (*3*) is plausible and would be done at the hardware calibration level.

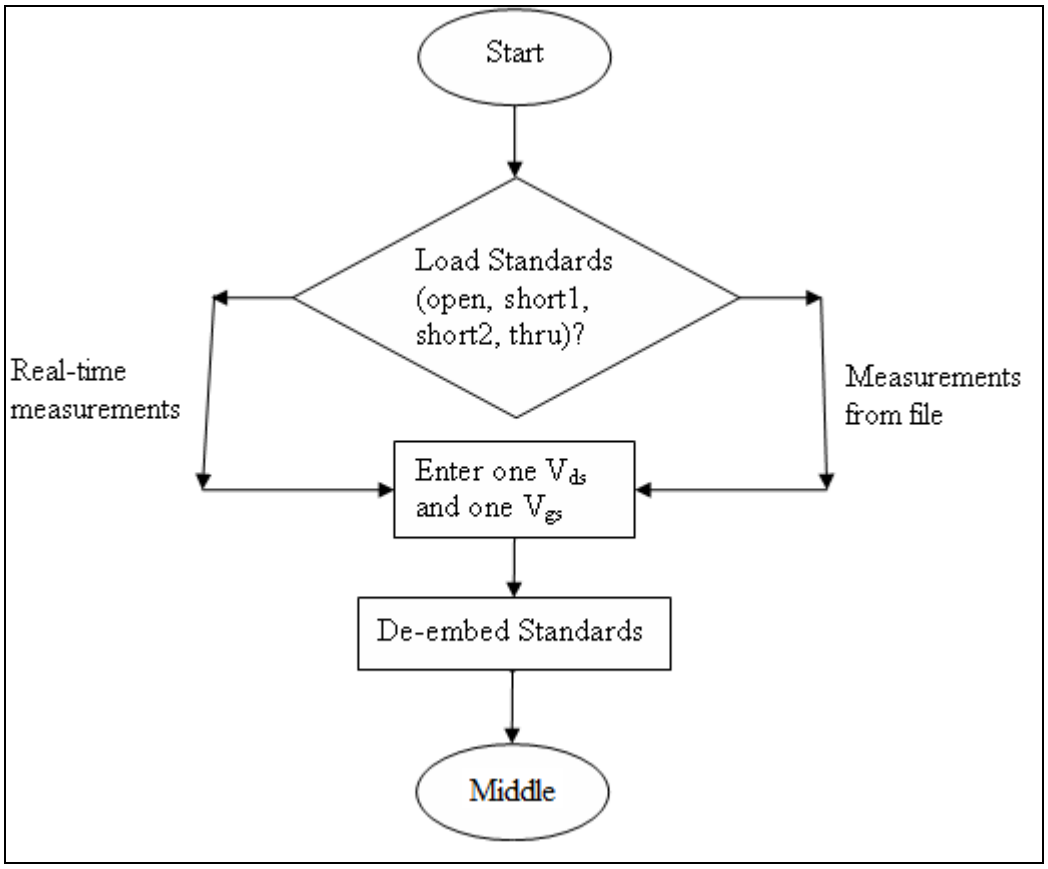

Figure 5. First half of H21 characterization flow chart.

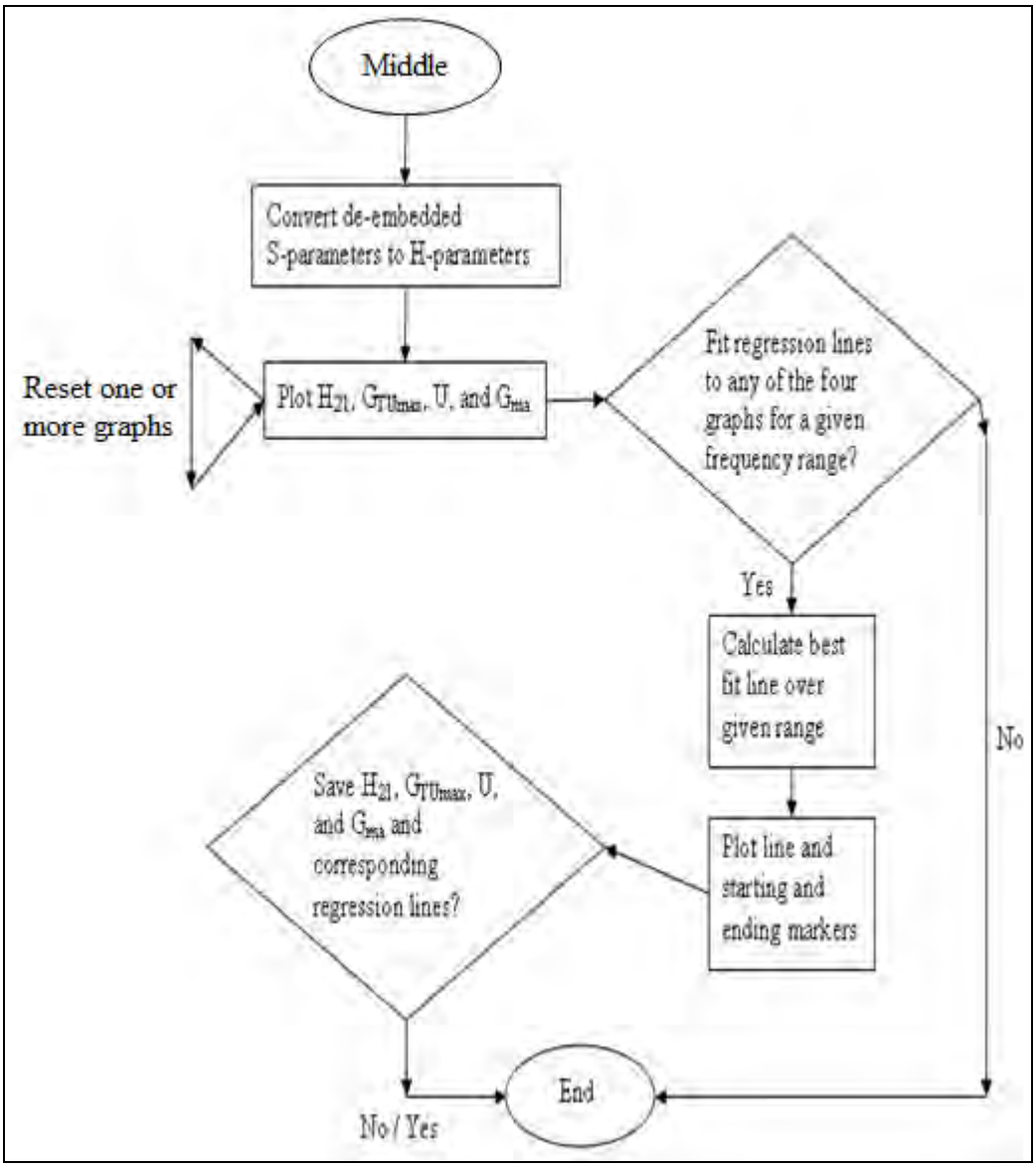

Figure 6. Second half of H21 characterization flow chart.

5. Verification of Hardware/Software

To verify the operation of both the hardware setup and the software itself, a Gallium Nitride (GaN) FET was characterized for both DC and RF operation. The device chosen is GHCD 500P_P175_1GS1P5GD and is illustrated in figure 7 as it appears on-wafer. One can locate it on wafer KC0051-07—contractor ID SC06-425, reticle R4C4, device ID 26—stored in Room 3D067 of Building 207. The generated DC characteristics are shown in figure 6, the family of I-V curves for the GaN FET. This output results from the I-V algorithm outlined and explained in the previous section. This particular FET has a small gate width (40 μm), therefore attributing to

the relatively small maximum I_{DS} value of the sweep (6 mA). In terms of gate width, larger transistors, which are not discussed in this documentation, naturally provide more current flowing through the channels.

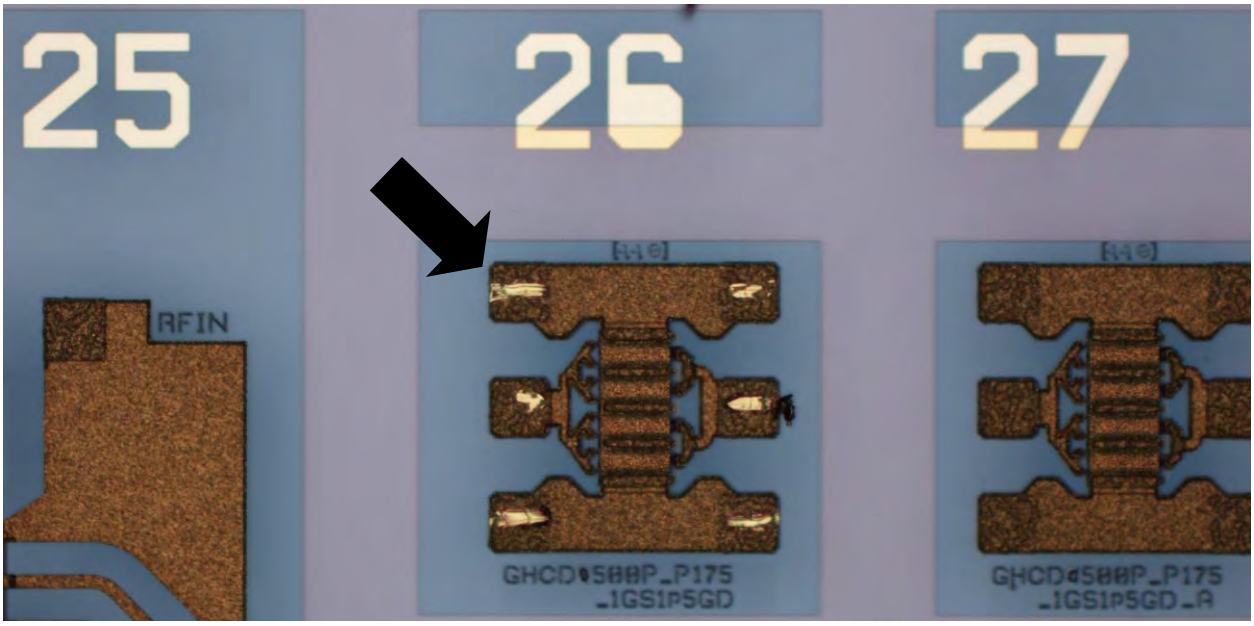

Figure 7. Tested GaN device GDCH_500P_P175_1GS1P5GD.

For the same DUT as before, the RF characteristics were produced by the software and are shown in figures 8 and 9. Figure 8 shows the transconductance curves with the proper fixed V_{DS} bias and indicates that the g_m peak for the GaN FET is 24.6062 mS. The V_{GS} value corresponding to that peak is –1.8 V. Figure 9 manifests the H_{21} characterization, showing the f_T for this device is 38.1 GHz; the f_{MAX} value converges between 69.8 GHz and 71.4 GHz. The user settings entered for this device to produce these curves is also show in figure 10.

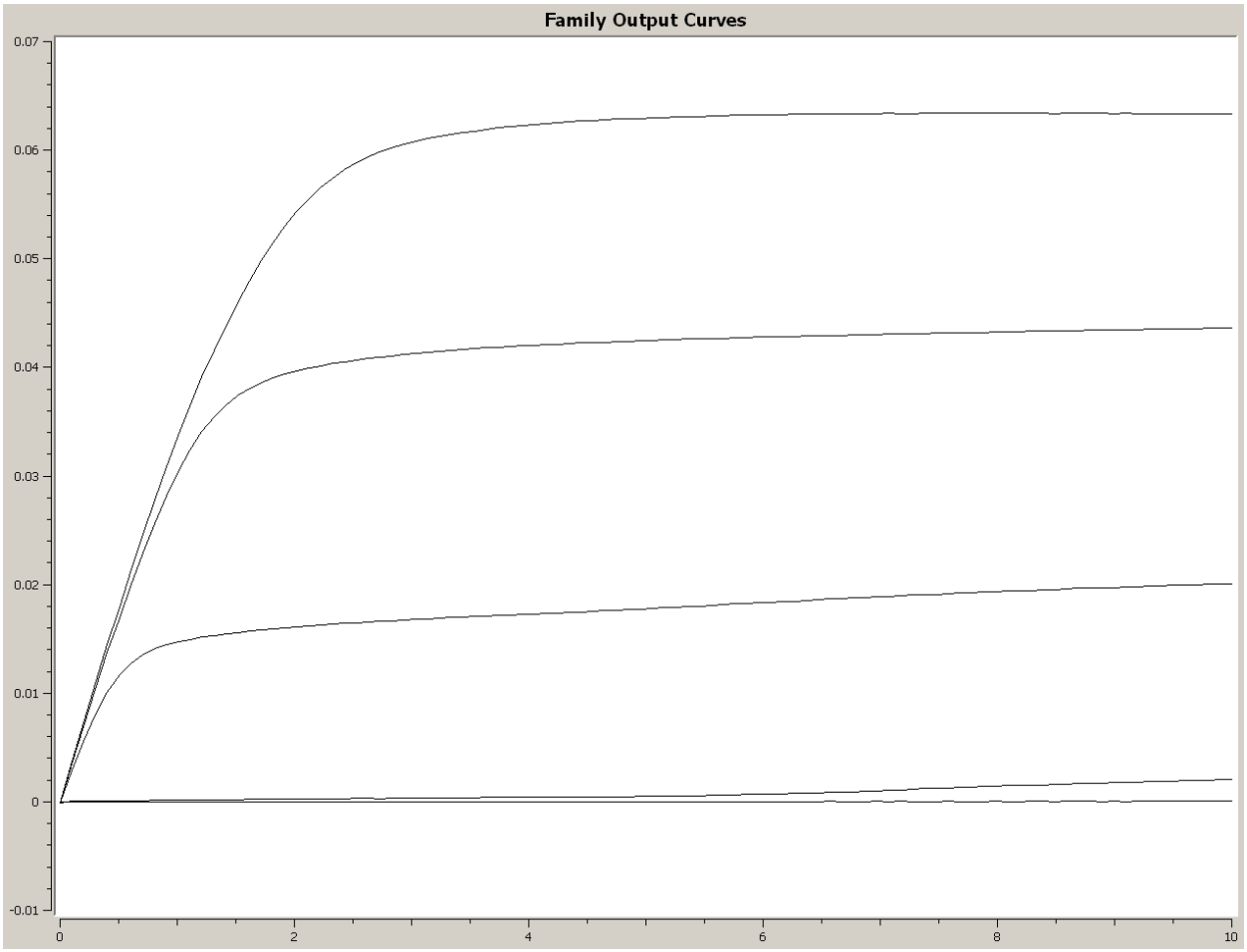

Figure 8. Example output I-V curves.

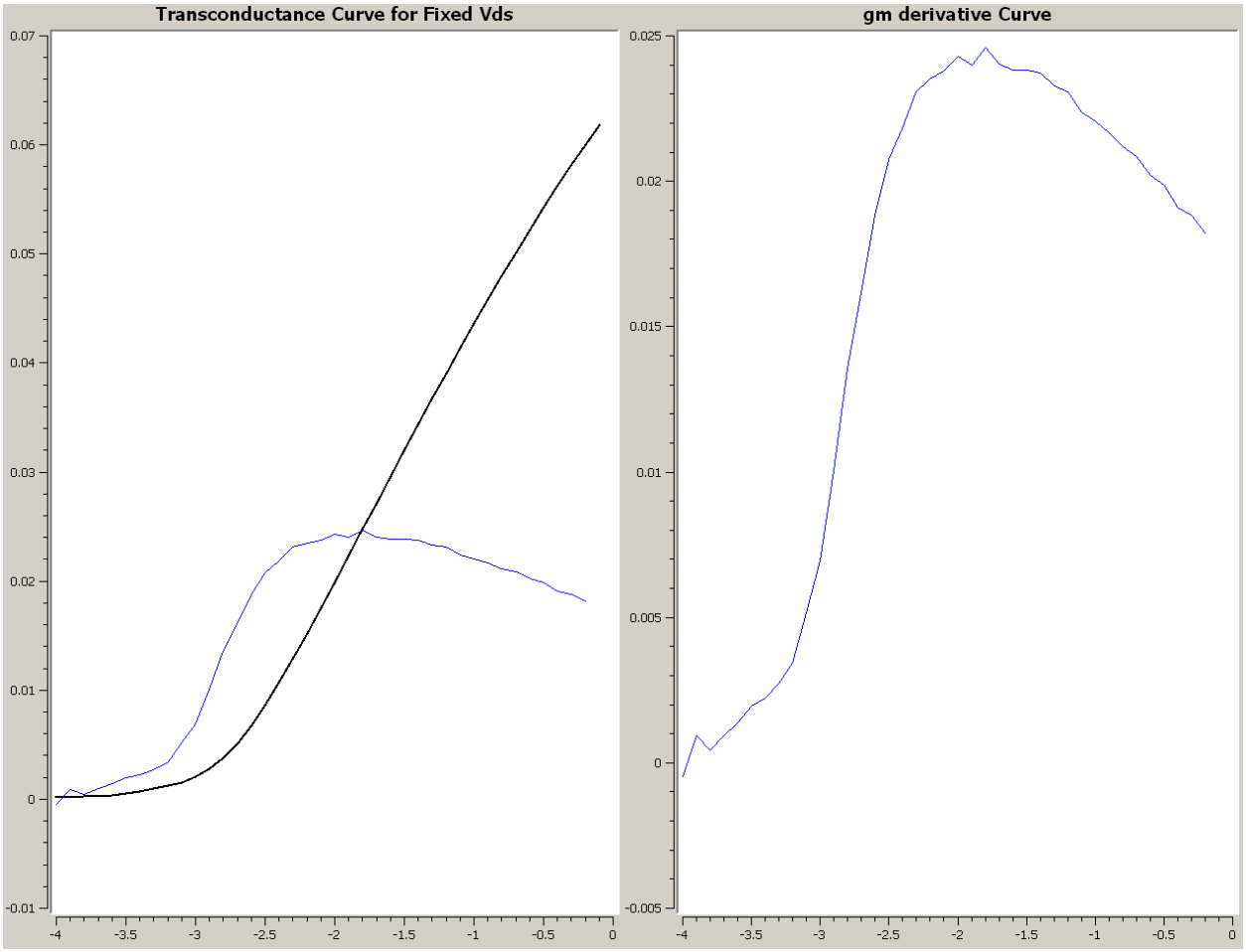

Figure 9. Example Transconductance measurements.

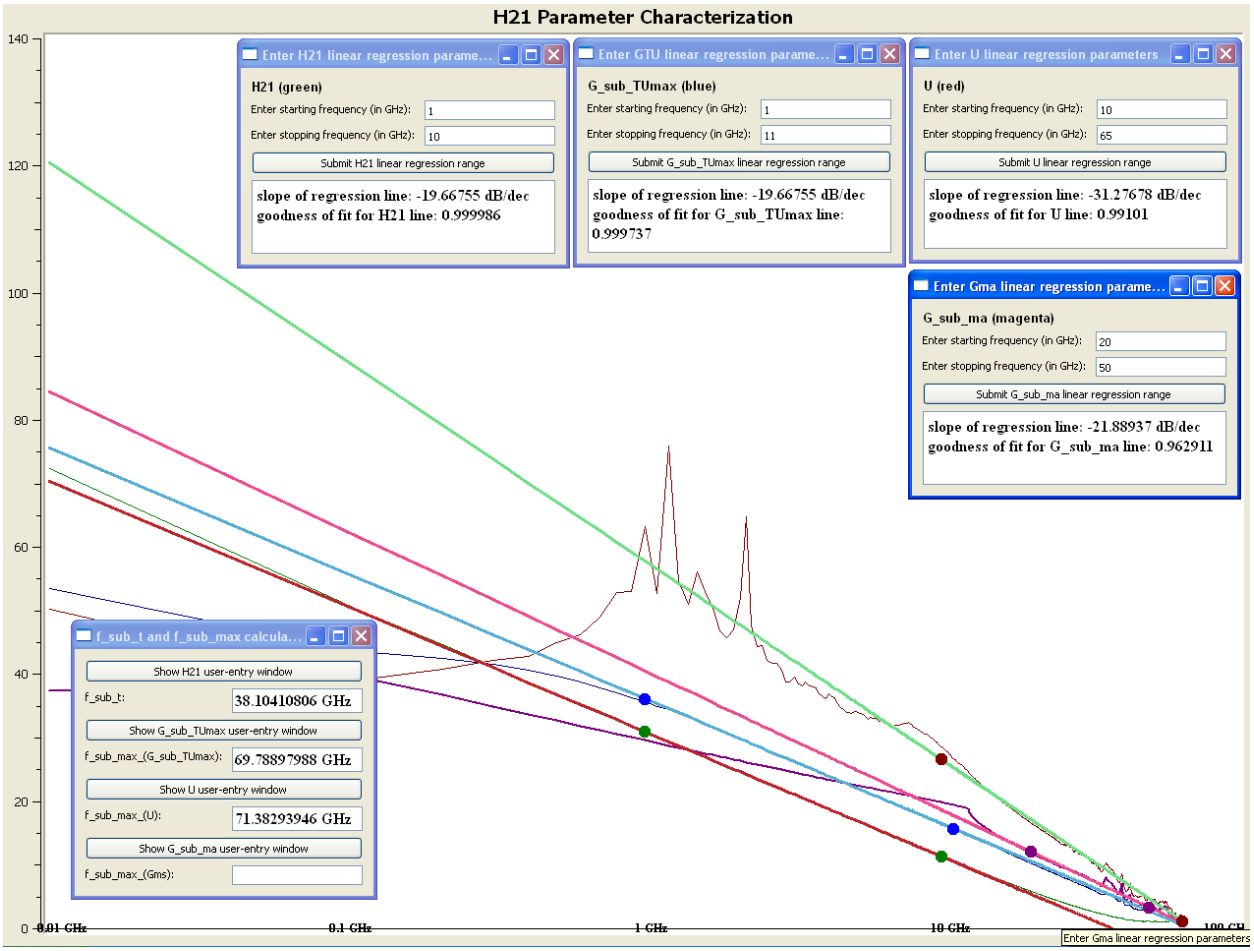

Figure 10. Complete H21 characterization environment.

6. Summary and Conclusions

Using one software tool that aids the user in accomplishing the task in three steps to characterize f_T and f_{MAX} is economic and pragmatic. Users can confirm their graphical results via looking at the G_{TUmax}, U, and G_{ma} curves and visually verifying if the three f_{MAX} values seem to approximate the same value. This type of device investigation is commercially available: Cascade Microtech implemented a more robust system called WinCal that aims, in part, to calculate f_T and f_{MAX} experimentally. However, this software solution is more economical and has a cleaner and more streamlined user interface.

Due to the limited nature of the experimental setup, further verification with more process technologies would be useful to perform to ensure robustness of this tool. However, similar analyses—obtaining I-V plots and f_T and f_{MAX} via transconductance and H_{21} characterization of any FET technology are possible. Some other common technologies that exist are Gallium

Arsenide (GaAs), Indium Phosphide (InP), Silicon Germanium (SiGe), Silicon (Si), and graphene. Once characterized, devices of the same technology can be compared; similarly, devices can be compared across technologies to learn more about geometry and technology qualities.

7. References

1. Vandamme, E. P.; Schreurs, D.M.M.-P.; Van Dinther, G. Improved Three-step De-embedding Method to Accurately Account for the Influence of Pad Parasitics in Silicon On-wafer RF Test-structures. *Electron Devices, IEEE Transactions on* **April 2001**, *48* (4), 737–742.

2. Cho, H.; Burk, D.E. A Three-step Method for the De-embedding of High-frequency S-parameter Measurements. *Electron Devices, IEEE Transactions on* **June 1991**, *38* (6), 1371–1375.

3. Williams, D. F.; Wang, J.C.M.; Arz, U. An Optimal Vector-Network-Analyzer Calibration Algorithm. *Microwave Theory and Techniques, IEEE Transactions on* **December 2003**, *51* (12), 2391–2401.

4. Agilent Technologies, "Technical Specifications Agilent Technologies PNA Series Network Analyzers E8361A/C" 08 January 2011. <http://cp.literature.agilent.com/litweb/pdf/E8361-90007.pdf>.

5. Pozar, David M. *Microwave Engineering*; Hoboken, NJ: J. Wiley, 2005. Print.

6. "Learn Simple/Linear Regression Tutorial, Definition, Example, Formula." *Free Online Math Calculator and Converter*. Web. 05 July 2011. <http://easycalculation.com/statistics/learn-regression.php>.

7. "WinCal XE Software: Cascade Microtech, Inc." *Welcome to Cascade Microtech: Cascade Microtech, Inc.:* Web. 05 July 2011. <http://www.cmicro.com/products/probes/wincal-xe>.

List of Symbols, Abbreviations, and Acronyms

DUT	device under test
FETs	field effect transistors
GaAs	gallium arsenide
GaN	gallium nitride
GPIB	general purpose interface bus
GSG	ground-signal-ground
GUIs	graphical user interfaces
InP	indium phosphide
I-V	current-voltage
RF	radio frequency
Si	silicon
SiGe	silicon germanium
UI	user interface
VNA	vector network analyzer

NO. OF COPIES	ORGANIZATION
1 ELEC	ADMNSTR DEFNS TECHL INFO CTR ATTN DTIC OCP 8725 JOHN J KINGMAN RD STE 0944 FT BELVOIR VA 22060-6218
1 CD	OFC OF THE SECY OF DEFNS ATTN ODDRE (R&AT) THE PENTAGON WASHINGTON DC 20301-3080
1	US ARMY RSRCH DEV AND ENGRG CMND ARMAMENT RSRCH DEV & ENGRG CTR ARMAMENT ENGRG & TECHNLGY CTR ATTN AMSRD AAR AEF T J MATTS BLDG 305 ABERDEEN PROVING GROUND MD 21005-5001
1	US ARMY INFO SYS ENGRG CMND ATTN AMSEL IE TD A RIVERA FT HUACHUCA AZ 85613-5300
1	COMMANDER US ARMY RDECOM ATTN AMSRD AMR W C MCCORKLE 5400 FOWLER RD REDSTONE ARSENAL AL 35898-5000
1	US GOVERNMENT PRINT OFF DEPOSITORY RECEIVING SECTION ATTN MAIL STOP IDAD J TATE 732 NORTH CAPITOL ST NW WASHINGTON DC 20402
8	US ARMY RSRCH LAB ATTN IMNE ALC HRR MAIL & RECORDS MGMT ATTN RDRL CIO LL TECHL LIB ATTN RDRL CIO MT TECHL PUB ATTN RDRL SER E S TROCCHIA ATTN RDRL SER E R DEL ROSARIO ATTN RDRL SER E T IVANOV ATTN RDRL SER E R PROIE ATTN RDRL SER E T FARMER ADELPHI MD 20783-1197